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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Cheng-Lien Chiang		
Assignee:	Bridge Semiconductor Corporation		
Title:	THREE-DIMENSIONAL STACKED SEMICONDUCTOR PACKAGE DEVICE WITH BENT AND FLAT LEADS AND METHOD OF MAKING SAME		
Serial No.:	10/695,564	Filed:	October 28, 2003
Examiner:	Williams, A.	Group Art Unit:	2826
Atty. Docket No.:	BDG005-6		

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION FOR WITHDRAWAL OF RESTRICTION REQUIREMENT

Dear Sir:

This Petition is filed under 37 C.F.R. § 1.144 to request that the outstanding restriction requirement be withdrawn.

I. FACTS

The captioned-application was filed on October 28, 2003. The original application contains claims 1-100.

The Office Action dated June 22, 2004, issued a restriction requirement. The Examiner's entire basis for restriction was as follows: "This application contains claims directed to the following patentably distinct species: Any one of the species or one set of the same species in figures 1A to 22."

The Response filed June 29, 2004, provisionally elected claims 1-60 and 91-100 (Figure 19) for prosecution on the merits. The Response also traversed the restriction requirement and requested that it be withdrawn. The arguments are repeated below.

The Office Action dated August 31, 2004, maintained the restriction requirement. The Examiner's entire basis for maintaining restriction was as follows: "The Examiner would be unduly burdened to evaluate all claims fully on their merit at the full time."

II. ARGUMENTS

Claims 1-100 are directed to a three-dimensional stacked semiconductor package device that includes (1) a first semiconductor package device including (a) a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces, (b) a first semiconductor chip within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad, and (c) a first lead that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad, wherein the first lead outside the first insulative housing is bent downwardly, (2) a second semiconductor package device including (a) a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces, (b) a second semiconductor chip within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad, and (c) a second lead that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat, and (3) a conductive bond outside the insulative housings that contacts and electrically connects the leads, wherein the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, and the first top surface faces towards the second bottom surface.

Thus, claims 1-100 are highly related to one another.

The claims correspond to the figures as follows:

Species	Figure	Claims
I	19	1-60 and 91-100
II	20	61-70
III	21	71-80
IV	22	81-90

Claims 1, 11, 21, 31, 41, 51 and 91 (Figure 19) are directed to a stacked device that includes first (lower) and second (upper) semiconductor package devices.

Claim 61 (Figure 20) is directed to a stacked device that includes first (lower) and second (upper) semiconductor package devices as well as a third semiconductor package device above the second semiconductor package device.

Claim 71 (Figure 21) is directed to a stacked device that includes first (lower) and second (upper) semiconductor package devices as well as a third semiconductor package device that extends into a cavity in the first semiconductor package device.

Claim 81 (Figure 22) is directed to a stacked device that includes first (lower) and second (upper) semiconductor package devices as well as a third semiconductor package device that extends into a cavity in the second semiconductor package device.

There must be a serious burden on the Examiner if the restriction is required (M.P.E.P. § 803). Where the related inventions as claimed are shown to be distinct, the Examiner, in order to establish reasons for insisting upon restriction, must show by appropriate explanation one of the following: (A) separate classification thereof; (B) a separate status in the art when they are classifiable together; or (C) a different field of search (M.P.E.P. § 808.02).

The Examiner has not even attempted to explain how examining the species I-IV would involve separate classification, separate status in the art, or a different field of search (M.P.E.P. § 808.02). Therefore, the Examiner has ignored mandatory elements set forth in the M.P.E.P. and the restriction requirement is improper.

The Examiner has the burden of establishing that the restriction requirement is justified. The mandatory elements set forth in the M.P.E.P. prevent the Examiner from having unfettered discretion over issuing restriction requirements that force Applicant to file divisional applications and absorb the related costs and delays in order to have the non-elected claims considered on the merits.

If, however, the Examiner can obtain a restriction requirement merely by asserting that "any one species or any one set of the same species in figures 1A to 22" and he would be "unduly burdened to evaluate all claims" then these mandatory elements are easily circumvented and rendered meaningless.

For these reasons, Applicant respectfully asserts that the restriction requirement is totally unjustified and requests that it be withdrawn.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 13, 2004

D Sigmond — 9/13/04

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Date of Signature

Respectfully submitted,

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